



ENABLER OF GREEN APPLICATIONS

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FACT BOX

NAME:	UltimateGaN - Research for GaN technologies, devices and applications to address the challenges of the future GaN roadmap.
START:	01 May 2019
DURATION:	42 Months
TOTAL COSTS:	~ EUR 48 Mio.
TOTAL PERSON MONTHS:	3846
CONSORTIUM:	26 partners from 9 countries
COORDINATOR:	Infineon Technologies Austria AG
WEBSITE:	www.ultimategan.eu



ACKNOWLEDGEMENT

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CONTACT

HERBERT PAIRITSCH
LISA ZERNIG

Infineon Technologies Austria AG
Siemensstraße 2
A-9500 Villach
Austria

UltimateGaN@infineon.com

THE PROJECT

The highly ambitious ECSEL project UltimateGaN consists of 26 partners from 9 European countries that strive to achieve significant improvement in digitising the European industry by means of GaN Electronic Components and Systems being used in applications, information highways and data centres in order to overcome the challenges of today's society.

Digitalisation and its underlying key technologies are an essential part of the answers to many of today's daunting challenges. Information highways and data centres are the "backbone" of the entire digitalisation and electrical Energy is the essential resource powering them (about 900 TWh were published for the "Internet" demand of 2012). Because of the increasing demand for data -traffic, -storage and -processing (average yearly increase of about 7%), higher energy efficiency of the energy management "backbone" is mandatory. These efficiency gains are also of a high value for energy conversion for renewables and mobility. Whenever silicon based semiconductors devices reach their limits, Gallium Nitride (GaN) based power semiconductors are promising candidates enabling much higher switching frequencies together with highest energy conversion efficiencies.

The economic necessity of making devices smaller while being even more reliable in every generation leads to severe upcoming challenges which demand fundamental research activities:

- Higher electric fields (Drift phenomena impacting lifetime)
- Higher current densities (Electro-migration impacting lifetime)
- Higher power densities (Thermal issues limiting the compactness potential)

Several FP7 and H2020 projects, among them the ECSEL pilot-line project "PowerBase" have proven these assumptions and serve as the basis for the availability of the first generation of European GaN-devices. Also the ability to

achieve more efficient and more compact applications by the use of GaN devices could be proven. But these projects also made clearly evident, that the challenges of the GaN technologies have been heavily underestimated. This results in a still very high potential of the GaN material system that waits to be explored leading to the necessity that the established IA pilot-line triggers a subsequent RIA-project.

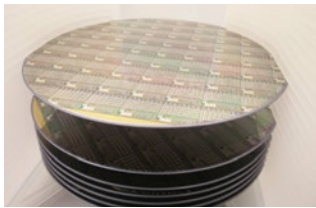
All these challenges are forming a "red brick wall" for the next GaN on Silicon technology generations and hamper shrinking of GaN devices which is necessary to improve the affordability of GaN-devices to introduce the outstanding performance of this material system into a wider range of applications. Beside the technical performance a distinct focus at next GaN on Si technology generations must be put on enhancing the cost competitiveness (in comparison to GaN on other substrates e.g. SiC), thus enabling higher volume as a base for economy of scale (leaving the vicious circle cost volume). This would multiply the effects of the energy saving capabilities of GaN-products.

OBJECTIVES AND RESULTS

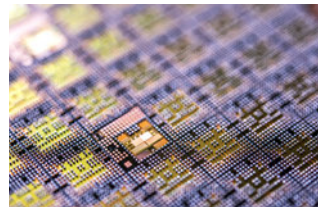
UltimateGaN will focus on the next generation of GaN technology, particularly addressing six major objectives along and across the entire vertical value chain of power and RF electronics, focusing on research and innovation in the fields of technology (including materials, equipment and device concepts), packaging, reliability and application.

UltimateGaN is a work package based project with strong interactions along the value chain whereas the results are demonstrated in relevant applications that enable digitalisation (5G) and energy efficient power conversion (Smart Grids, Smart Mobility) to safeguard Europe's leading position in high performance power and RF applications. This spans expertise from industry and research along the dimensions of Vertical Power GaN, Benchmark

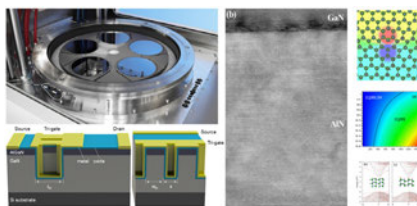
Lateral Power GaN, GaN on Silicon RF Break Through, Assembly and Packaging of high speed and high frequency GaN on Si devices, GaN Reliability and Defect Research and GaN RF and Power Applications. The UltimateGaN results are demonstrated in relevant industrial Use Cases enabled by the value chain. The project partners will together create a unique value to foster energy efficiency and digitalisation.



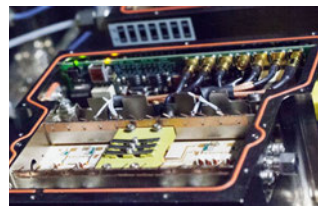
Objective 1: Research on vertical power GaN processes and devices pushing performance beyond current state-of-the-art



Objective 4: Braking the packaging limits – size, electrical and thermal constraints – for high performance GaN power products



Objective 2: Research on lateral GaN technologies and devices to achieve best in class power density and efficiency while optimizing cost vs. performance



Objective 5: Close the reliability and defect density gap for most innovative GaN devices



Objective 3: Bringing GaN on Silicon RF performance close to GaN on Silicon Carbide thus enabling an affordable 5G rollout



Objective 6: Demonstrate European leadership in high performance power electronics and RF application domains

#1 RESEARCH ON VERTICAL POWER GAN PROCESSES AND DEVICES PUSHING PERFORMANCE BEYOND CURRENT STATE-OF-THE-ART

>13 μm -thick GaN grown by MOCVD on 200 mm engineered substrates with a poly-AlN core as a route towards manufacturable vertical GaN devices.

Within work package 1 of UltimateGaN, promising technologies for vertical GaN device manufacturing are being investigated. For these devices the electric field is directed vertically over the GaN device stack. Due to that the target breakdown voltage does not impact the device footprint, which makes it a very suited technology for high voltage applications. Within the project we focus on the carrier substrate choice for reduced device production cost with attention to the defect densities within the GaN layers grown on top of the different substrates.

To achieve a low defect density in the GaN device layers ($<10^7 \text{ cm}^{-2}$), homo-epitaxial growth on GaN substrates is preferred. Furthermore, HVPE grown drift layers can significantly reduce the total growth time for the GaN stacks, when using thick drift layers. A fast growth rate HVPE process is under development by NaMLab. For GaN-on-GaN devices, the substrate cost is very high and the available substrate size is still limited, with most research performed on 50 mm-diameter substrates today.

We propose two technologies that can make vertical devices manufacturable on large scale diameter substrates. Si substrates are low in cost, but due to the mismatch in thermal expansion and lattice constant to GaN, the wafers become

fragile when thick GaN stacks are grown on large diameter substrates. Coalescence of epitaxial nanowires into a planar film decouples the device stack from the growth-substrate and therefore does not have the same material limitations of generic GaN-on-Si technology. This technology is provided by subcontractor Hexagem AB. Experiments have confirmed the underlying mechanisms of this effect, with a 4.1- μm -thick device layer being grown on a GaN-on-Si template buffer. Modeling predicts that 10-12 μm thick drift layers on 200-mm-diameter substrates are possible. Another cost-effective substrate choice, although more expensive compared to Si is an engineered substrate with a poly-Aluminum Nitride core, namely QST[®]. The substrate with a closely matched coefficient of thermal expansion to GaN allows the growth of thick GaN stacks on SEMI standard thickness 200 mm substrates. The GaN device manufacturing has been performed by imec within the project. GaN stacks of > 13 μm have been grown by metal-organic chemical vapor deposition in an AIXTRON G5+ C reactor, including a 10 μm -thick drift layer. During the full device manufacturing using stacks with a 5 μm -thick drift layer on 200 mm-diameter substrates, no wafer breakage occurred. Due to the observed mechanical robustness of the substrates, they are an excellent choice for fabrication of vertical GaN devices.



200 mm GaN-on-QST[®], with processed trench gate MOSFET devices

#2 RESEARCH ON LATERAL GAN TECHNOLOGIES AND DEVICES TO ACHIEVE BEST IN CLASS POWER DENSITY AND EFFICIENCY WHILE OPTIMIZING COST VS. PERFORMANCE

Lateral GaN Power Devices will reach exceptional performance and cost levels with novel epitaxy and device concepts. Record figure-of-merit achieved!

In UltimateGaN work package 2, ten consortium partners from five European countries have been joining their forces to strive for the next levels of performance and cost improvement for lateral GaN power technologies. Ultra-compact and best-in-class 100 and 600V normally-off GaN power HEMTs have been realized on 200mm Silicon substrates resulting in a substantial productivity increase compared to state-of-the-art 150mm technologies.

One main focus was the improvement of the underlying 200mm GaN-on-Si epitaxial processes, including design optimization of reactor hardware. In another activity most advanced metallization schemes have been implemented, enabling interconnects to be placed directly on active transistor area and with this achieving a massive device shrink. Metallization and interconnect robustness has been investigated with most powerful tools such as Giga-Hertz Scanning Acoustic Microscopy and Nano-Indentation, leading to best design and material choices.

Furthermore, revolutionary buffer-free GaN-on-SiC epitaxy concepts have been driven forward and scaled from 100mm to 150mm wafer diam-

eter. For SiC substrate cost reduction, in-house SiC crystal growth and wafer production have been pursued while optimizing growth equipment and wafering processes. A manufacturing line for GaN HEMTs has been established to benchmark GaN-on-SiC in comparison to GaN-on-Si epitaxy. Atomistic simulations based on quantum mechanical calculations and material analysis with transmission electron microscopy as well as advanced cathodoluminescence spectroscopy provided novel insights into the behavior of GaN epitaxy and crystal defects.

Cutting-edge research on tri-gate device concepts was pursued and resulted in unprecedented specific on-state performance. Devices with several 2DEG channels (2DEG = Two-Dimensional Electron Gas) stacked on top of each other achieved a record figure-of-merit (FoM) of 4.6 GW/cm². With this, lateral GaN devices surpassed the FoM limit of 4H-SiC semiconductors for the first time.



Fully processed 200mm GaN-on-Si wafer with power HEMT devices

#3 BRINGING GAN ON SILICON RF PERFORMANCE CLOSE TO GAN ON SILICON CARBIDE THUS ENABLING AN AFFORDABLE 5G ROLLOUT

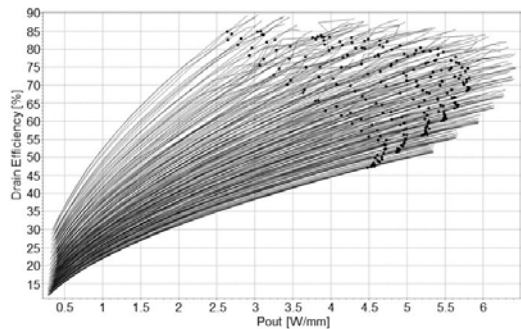
RF power GaN on silicon technology delivering on ist promises of large scale 8" silicon-level manufacturing and GaN on silicon carbide level performance.

GaN HEMTs on Silicon wafers for RF applications (GaN-Si) have been pursued since more than 20years to reduce the very high cost of the state-of-the-art technology GaN-SiC. So far GaN-Si has not been widely used due to significantly lower performance compared to GaN-SiC. The combination of performance and cost requirements are most critical at mm-wave frequencies where high performance monolithically integrated circuits are needed. We have developed a novel GaN-Si technology on 8" to deliver on the full potential of RFGaN on silicon, to provide performance similar to GaN on SiC but at much lower cost.

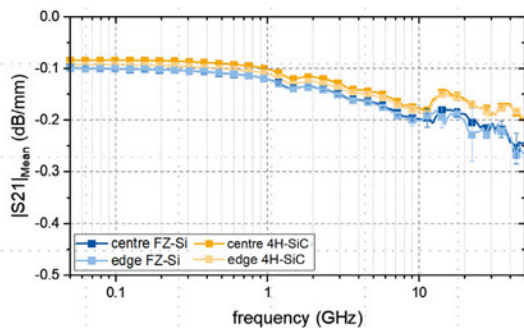
One of the major drawback of GaN-Si so far has been the higher losses due to the silicon substrate translating into lower efficiencies especially at high frequencies. In Fig.1 the efficiency of an GaN-Si transistor measured by load pull is shown. The graph shows drive-up curves versus output power for different load impedances at 3.5GHz. The transistor is showing the feasibility of our newly developed within Ultimate-GaN. The achieved efficiencies of over 85% are amongst the highest reported for AlGaN HEMTs, including GaN-SiC.

The losses associated with the substrate are typically significantly higher for Silicon com-

pared to Silicone Carbide. In order to maintain high transistor efficiencies at even higher frequencies the substrate losses for GaN-Si have to be reduced. In Fig. 2 transmission line losses are shown on SiC and Si. We were able to reduce the losses significantly and get close to the losses observed on SiC. These improvements provide the basis to scale the technology to achieve close to GaN-SiC efficiencies also at frequencies above 20GHz.



Loadpull efficiency versus Output power at 3.5GHz for various load impedances



Transmission line loss versus frequency on Si and SiC substrates

#4 BRAKING THE PACKAGING LIMITS – SIZE, ELECTRICAL AND THERMAL CONSTRAINTS – FOR HIGH PERFORMANCE GAN POWER PRODUCTS

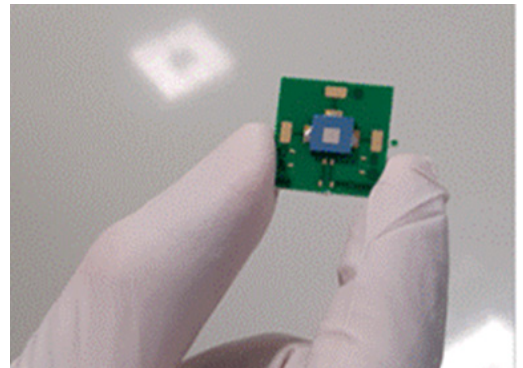
Packaging and integration technologies are key to bring GaN power on the road.

GaN FETs enable significantly increased power densities due to the high charge carrier mobility in the 2DEG (Two-Dimensional Electron Gas) channel. Together with very high switching frequencies they bring the basis for low loss energy conversion. However, these properties can only be harvested if the electronic package offer lowest parasitics not limiting the full capability of the GaN switch. Thus, achievement lowest parasitic impedance is the general theme of the work package 4 towards all use cases developed.

One particular example is the innovative approach of plateable mold where 2 parallel GaN switches are densely packaged realizing half RDSon values and a very low inductive impedance due to wirebond-less interconnects. A dedicated System in Package approach for combine GaN driver and switching stage is developed for a LiDAR sensor, where a nanosecond short pulses are required to ensure eye safety despite high pulse currents to reach long range. In the field of packaging for 5G applications low parasitics are reached with the investigation of PCB embedding, where the GaN device is directly embedded inside the PCB facilitating very short interconnect distances.

In UltimateGaN work package 4 partners contribute to package innovations that improve overall switching performance of GaN devices,

miniaturize size and improve thermal dissipation. Both product and process innovation is generated last but not least with aspects of additive manufacturing where packages can be directly tune to the device and application with a high degree of flexibility. As GaN devices are impacting on higher power density at low size a special emphasis was given on multi-domain simulations to calculate electrical, thermal and thermomechanical behavior in one approach, as the different domains are completely coupled.



UltimateGaN addresses three fields of applications

#5 CLOSE THE RELIABILITY AND DEFECT DENSITY GAP FOR MOST INNOVATIVE GAN DEVICES

Advanced research, from defect characterization to degradation physics, from failure analysis to application-level reliability.

Advanced GaN devices have unique features, compared to the conventional silicon counterparts: the electric fields in GaN can be up to 10 times higher than in silicon; in addition, the operating temperature range is wider than that of conventional electronics, and this permits to increase power density (ideal for end users). Temperature and electric field can be driving forces for degradation, and a detailed research on GaN reliability and related defects is the key for a successful development of gallium nitride technology.

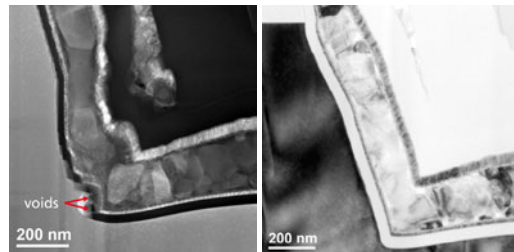
The WP5 of UltimateGaN generated a number of highly innovative results in the field of GaN reliability and defect research, thanks to the collaboration of 18 partners, that worked on different levels, from the development of innovative methodologies for defect characterization to material-level defect analysis, all the way to device-level stability investigation, and application-level testing.

SEVERAL KEY RESULTS HAVE BEEN OBTAINED, INCLUDING:

- 1) identification of the physical processes that limit the reliability of semi-vertical GaN devices, with consequent optimization of the gate stack, of the annealing procedures, and minimization of the leakage components;

- 2) understanding of the charge-trapping phenomena in lateral power HEMTs, with analysis of the impact of doping and V/III ratio on device performance, and description of the positive and negative charge-storage processes;
- 3) identification of the degradation modes in RF GaN devices, and analysis of accelerated stress tests, under different bias/temperature conditions;
- 4) detailed analysis and modeling of packaged/ assembled GaN devices, supported by FE simulation and IR camera analysis;
- 5) description of degradation in application conditions, identification of the related causes of GaN failure, and of solutions strategies.

The results obtained in WP5 have been used within the other WPs for a successful improvement in device performance and reliability.



STEM analysis of defective gate formation and improved gate architecture

#6 DEMONSTRATE EUROPEAN LEADERSHIP IN HIGH PERFORMANCE POWER ELECTRONICS AND RF APPLICATION DOMAINS

By the use of last generation GaN devices, the RF power amplifiers and power converters will achieve several improvements on system performance, such as higher efficiencies, higher power densities and higher operation frequencies.

The objective of WP6 is to achieve benchmark performance in different RF and power applications, also evaluating the benefits of the GaN devices developed in the project. The technologies and the challenges in each domain are completely different:

- 1) For telecom and data centers application, the developed 2kW/48Vdc rectifier is based on IP65 fan-less design thank to low power losses of GaN devices. The demonstrator presents very good performance results, achieving an efficiency above 97%.
- 2) For RF frontends and radar, a Doherty style amplifier has been selected as the core of a 5G RF amplifier demonstrator. Measurements carried out with GaN-Si devices with wire-bonded PCBs will provide information to optimize and design a flexible demonstrator.
- 3) The challenge of LIDAR applications is to be able to provide a very short high current pulse, around 50A with a duration below 5ns.
- 4) For battery charger for PHEV/EV, two different approaches and demonstrators. A contact on-board charger with a high-ef-

iciency and high-power density has been developed thanks to GaN devices. In the case of the wireless battery charger, an integrated low-profile battery charger has been developed, increasing system efficiency and avoiding the wallbox.

- 5) A fully GaN 10kW single-phase photovoltaic inverter demonstrator has been developed based on new GaN modules, increasing the power density and reducing the cost of the system.
- 6) Several isolated DC/DC converters have been developed to integrate in a DC micro-grid, to interconnect different renewable energy sources with loads and energy storage systems. Long tests in field conditions are providing interesting results in terms of reliability in a real application.



UltimateGaN addresses three fields of applications

INNOVATIONS: TECHNOLOGY

ROUTE TOWARDS MANUFACTURABLE VERTICAL GAN DEVICES ON LARGE DIAMETER ENGINEERED SUBSTRATES

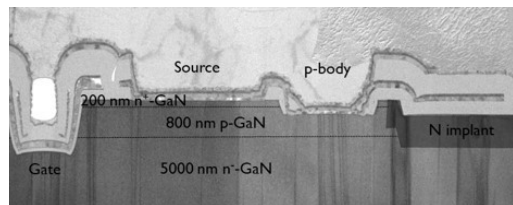
LEAD PARTNER / AUTHOR:

imec / Karen Geens

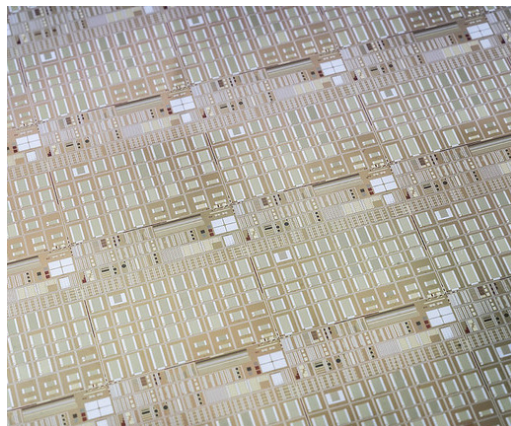
Trench gate MOSFET devices fabricated on 200 mm diameter engineered substrates with a poly-AlN core on > 8 μm GaN epitaxy, using a CMOS compatible process flow.

For on-wafer device fabrication it is beneficial to select a large diameter carrier substrate, in a production line to decrease the process cost. On top of the selected carrier substrate the epitaxial GaN layer growth is initiated after which trench gate MOSFET devices are processed. The number of fabricated devices will be higher for a substrate with a larger diameter while keeping the amount of processing steps the same. For vertical GaN devices most research today is on GaN substrates with limited substrate size and high cost. For this work we have selected engineered substrates with a poly-Aluminum Nitride core, namely QST®. The substrate with a closely matched coefficient of thermal expansion to GaN, allows the growth of thick GaN stacks on SEMI standard thickness 200 mm substrates, which are further scalable to 300 mm. The substrate cost is expected to approach the price of a standard SOI substrate by 2025. This choice allows to manufacture vertical devices CMOS compatible in a production line. Multi-finger semi-vertical trench gate Metal-Oxide-Semiconductor FET devices (Effective gate width = 60 nm) were fabricated, as test vehicle on a GaN stack > 8 μm , grown by Metal-or-

ganic chemical vapor deposition in a AIXTRON G5+ C reactor, including a 5 μm -thick drift layer. A good crystal quality as well as a good control of the wafers bow was obtained. The mechanically very strong substrates showed no wafer breakage during the full device processing. Trench gate MOSFET devices with an RON as low as 11 m Ω cm² were obtained, using a 2.5 nm Al₂O₃ and 100 nm SiO₂ bi-layer gate dielectric. The pn⁻-diode part of the stack reaches 550 V in reverse bias, for a 5 μm -thick drift layer with 2×10^{16} Si/cm³ doping.



TEM image of trench gate, source, p-body and device edge termination



Zoom in processed wafer

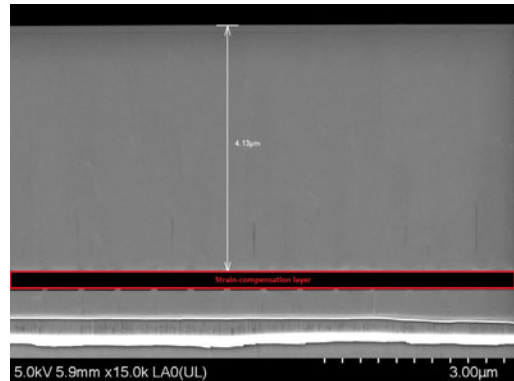
LARGE DIAMETER GAN-ON-SI WAFERS BY COALESCED NANOWIRE EPITAXY FOR SEMI-VERTICAL POWER DEVICES

LEAD PARTNER / AUTHOR:
RISE / Martin Berg

GaN on silicon for high-power electronic devices promoting sustainable transportation in the green economy. GaN on silicon for high-power electronic devices promoting sustainable transportation in the green economy.

One possible route to produce high-quality and large diameter GaN-on-Si wafers, necessary for low-cost high-voltage vertical devices, in a cost-efficient way is by subcontractor Hexagem AB's technology of coalescence of epitaxial nanowires into planar films. Within Ultimate-GaN, single-exposure full wafer lithography and etching processes for <110 nm holes 3 % hole-to-hole-variations in a SiNx-growth mask have been developed with the intent of establishing a scalable platform to reach large-diameter GaN-on-Si wafers. From these holes, GaN nanowires are epitaxially grown and merged into a planar epitaxial film with reduced dislocation density as compared to commercially available substrates. This is an effect of the device-structure being decoupled from the growth-substrate and therefore not as affected by the material limitations of generic GaN-on-Si technology. This technology allows for fabrication of thick GaN layers, which is required for high-voltage vertical devices on Si. Experiments have confirmed the underlying mechanisms of this effect, with a 4.1- μm -thick device layer being grown on a GaN-on-Si template buffer. The device layer

has a threading dislocation density on the order 10^8 cm^{-2} , and a root mean square roughness of < 0.4 nm. This result lay the foundation for growth and electrical characterization of thicker layers by breakdown measurement on semi-vertical diodes and in the scaling to larger wafer diameters, where modeling predicts that 10-12 μm thick crack-free drift layers on 200-mm-diameter is obtainable.



Cross-sectional scanning electron micrograph of a 4.1- μm -thick drift layer grown on top of a 300-nm-thick nanowire coalescence layer that also serve as strain compensation layer. The coalescence layer is blocked for IP protection.



Photograph of a crack-free GaN-on-Si 2" wafer with 4.1- μm -thick drift layer grown using the nanowire coalescence technology

MULTI-CHANNEL NANOWIRE DEVICES FOR EFFICIENT POWER CONVERSION

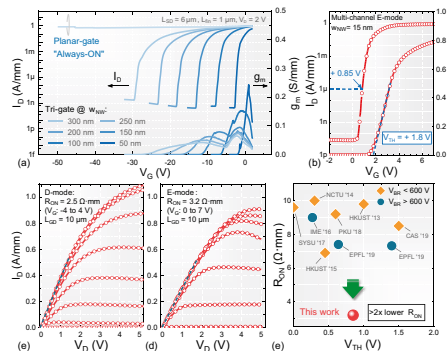
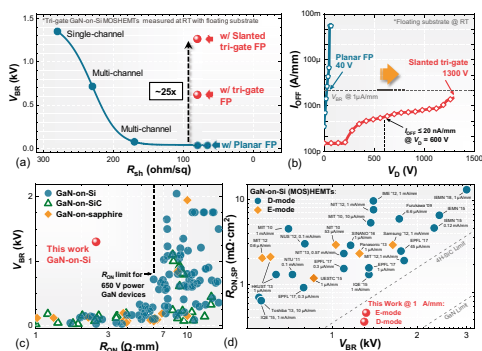
LEAD PARTNER / AUTHOR:

EPFL / Luca Nela and Elisa Matioli

Multichannel power devices made exhibited low specific on resistances of $0.46 \text{ m}\Omega \text{ cm}^{-2}$, enhancement-mode operation, improved dynamic behaviour and breakdown voltages as high as $1,300 \text{ V}$, resulting in a state-of-the-art figure of merit of 3.8 GW cm^{-2} .

Nanowire-based devices can potentially be of use in a variety of electronic applications, from ultrascaled digital circuits to 5G communication networks. However, the devices are typically restricted to low-power applications due to the relatively low electrical conductivity and limited voltage capability of the nanowires. In this project, EPFL showed that wide-band-gap AlGaIn/GaN nanowires containing multiple two-dimensional electron gas channels can be used to create high-electron-mobility tri-gate transistors

for power-conversion applications. The multiple channels lead to a significantly improved conductivity in the nanowires. Despite the high carrier density of $3.9 \times 10^{13} \text{ cm}^{-2}$, a V_{TH} of $+1.8 \text{ V}$ extracted by linear extrapolation of the ID-VG curve (or $+0.85 \text{ V}$ at $1 \mu\text{A mm}$) was achieved, along with a low I_{OFF} of only 57 pA mm at $V_G = 0 \text{ V}$ and a high ON/OFF ratio over 10^{10} , revealing excellent e-mode operation and tri-gate control over the multiple channels. The combination of tri-gated nanowires and multi-channel structures led to extremely low specific on resistances of $0.46 \text{ m}\Omega \text{ cm}^{-2}$ with enhancement-mode operation. This resulted in a more than a two-fold reduction in the on-resistance with respect to the best performing single-channel e-mode power device with similar V_{TH} . To reach large voltages, A slanted nanowire termination was introduced which resulted in breakdown voltages of 1300 V (below $1 \mu\text{A/mm}$), along with a small I_{OFF} below 20 nA/mm at $V_D = 600 \text{ V}$. The multi-channel devices achieved a record figure-of-merit of 4.6 GW/cm^2 that is substantially improved with respect to the single-channel counterpart. This is the first time that GaN lateral devices surpass the figure-of-merit limit of 4H-SiC semiconductors.



Nela, L., et al. "Multi-channel nanowire devices for efficient power conversion." Nature Electronics 4.4 (2021): 284-290

100V GAN-ON-SI POWER HEMT TECHNOLOGY IN 200MM WITH 3D INTERCONNECT

LEAD PARTNER / AUTHOR:

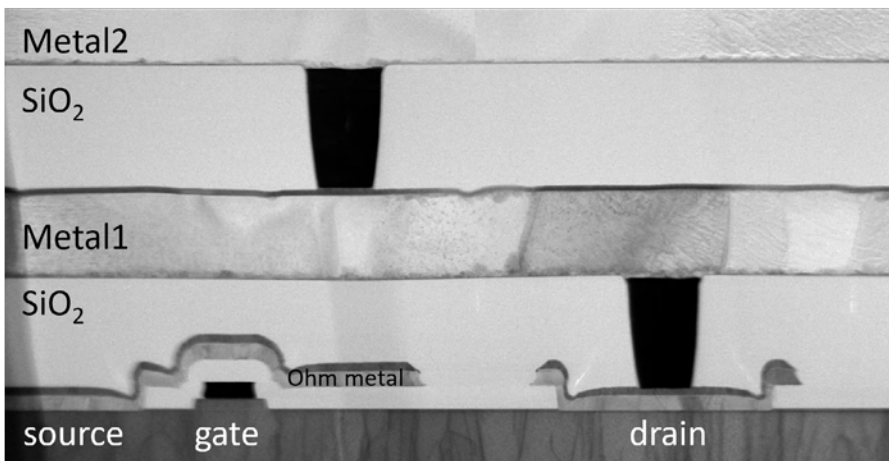
imec / Niels Posthuma

p-GaN gate HEMTs for low voltage applications with low on-resistance passing on-wafer reliability tests.

LIDAR (Light Distancing and Ranging) is an active remote sensing technology that uses light in the form of a pulsed laser to measure distance. LIDAR is a useful technology for many industries, from forestry to autonomous vehicles. This technology requires high power devices, for which GaN based enhancement mode High Electron Mobility Transistors (HEMTs) are well suited to be used in the driver circuit. The power devices should have a fast commutation speed, meaning that it is im-

portant for these devices to be compact and have a low on-resistance R_{on} , along with an advanced front-side interconnect scheme enabling low package inductances.

Within the UltimateGaN project imec has developed dedicated low-voltage e-HEMTs for the LIDAR driver circuit. The development includes all aspects of the design and fabrication process, from device design and layout using 3-dimensional interconnect technology, development of the epitaxial layer stacks, selection of the gate architecture, scaling of the gate structure and ohmic contacts, and development of a novel compact back-end structure with full planarization. The realized power HEMTs have a low typical R_{on} of 40 m Ω , a threshold voltage of 2.5V and a dynamic R_{dson} dispersion well below 20%. The power HEMTs pass the on-wafer High-Temperature Reverse Bias (HTRB) reliability test at a drain voltage of 100V.



Annular bright-field scanning transmission electron microscopy (ABF-STEM) micrograph of the realized scaled low-voltage e-HEMT for LIDAR applications

AIXTRON PROVIDES FULLY AUTOMATED MOCVD PLATFORM WITH WAFER HANDLING CAPABILITY UP TO 600°C

LEAD PARTNER / AUTHOR:

AIXTRON SE / T. Anders, N. Muesgens, H. Hahn, D. Fahle and M. Heuken

Throughput and performance optimized MOCVD platform using fully automated cassette-to-cassette wafer handling.

Within Ultimate GaN AIXTRON SE worked together with Infineon with the target to develop 200mm GaN on Si epitaxy processes with drastically higher throughput and reduced consumable costs. Spare parts with higher durability and life-time will be designed to minimize tool down times and cost. These activities are car-

ried out on the AIXTRON G5+ system at Infineon Villach as well in the AIXTRON lab in Herzogenrath. A big pool of characterization possibilities has given a substantial contribution to reach the first steps in the fields of process definition, cost down measures and system stability for this new 200mm power HEMT technology.

As a result, beyond the current state-of-the-art investigation, was shown on an AIXTRON G5+ cassette-to-cassette system (see figure) test at the site Villach to establish and validate the anticipated throughput increase. A stable handling capability operation was shown at 600°C in Infineon's production surrounding. To get there, problems in the system stability had to be solved by Infineon's and AIXTRON's experts. Due to this finding the timeframe for production and cleaning process cycles can be reduced by more than 30%.



Example picture of two AIXTRON G5+ process modules connected with a cassette to cassette handling system

NANOPIPES AND V-PITS: FORMATION MECHANISMS REVEALED FROM FIRST PRINCIPLES

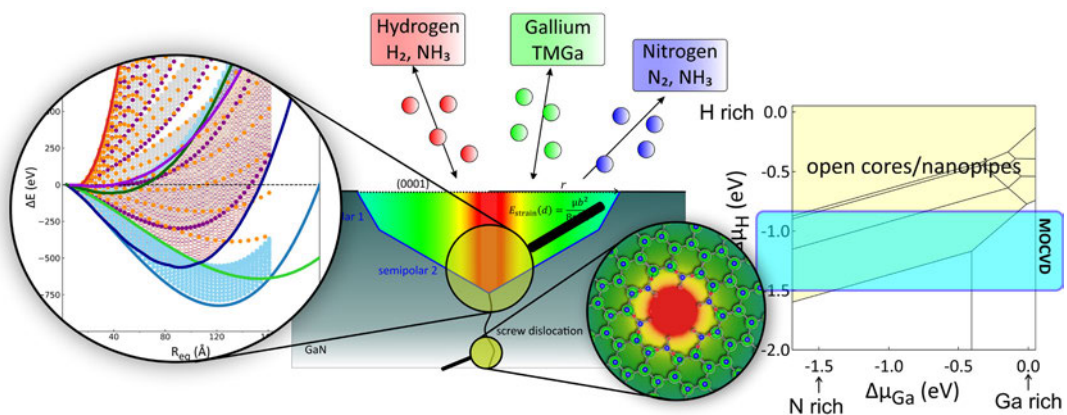
LEAD PARTNER / AUTHOR:
MPIE / Liverios Lymperakis

Revealing the origin and properties of detrimental extended defects from first principles: A route toward higher materials' quality.

Defects are imperfections and interruptions in the regular arrangement of the atoms in the crystalline solid. Defects have a strong impact on the properties of materials. Among them dislocations, i.e., extended 1D crystallographic irregularities, constitute a long standing and highly debated issue in the field of III-Nitride materials. Their effect on the materials' electronic properties is detrimental and they are considered to reduce the efficiency and reliability of power electronic devices. These defects are also strongly related to the formation of nanopipes, i.e., cylindrical hollow regions in the bulk, and

V-pits, i.e., inverted pyramids formed at surfaces or interfaces. Despite their technological importance, the root cause of both nanopipes and V-pits in GaN is not fully understood. Moreover, due to the peculiar character of these defects, experimental investigations at the atomistic level are challenging and not straightforward.

Within UltimateGaN, quantum mechanical calculations are combined with elasticity theory and thermodynamics to investigate the complex interplay between strain and surface energies which governs the formation and properties of these defects. Furthermore, their interaction with different growth environments is explicitly considered and the role of chemical species present during growth is identified. Our calculations provide an on-atomic-scale understanding of the formation mechanisms and reveal that these defects may spontaneously form under typical growth conditions. Nevertheless, the dependence of their properties, e.g., equilibrium radius or decoration by impurities, on the growth conditions constitutes a key output that can be employed in the growth design of these materials.



Schematic representation of a screw dislocation and a V-pit bounded by two different semipolar facets

HIGH PERFORMANCE AND COST-COMPETITIVE POWER HEMTs ON BUFFER-FREE GaN-ON-SiC WAFERS

LEAD PARTNER / AUTHOR:
RISE / Qin Wang

Large wafer scale fabrication of high-performance HEMTs on buffer-free GaN-on-SiC substrate enables its competitiveness in cost-sensitive RF and power electronics market.

GaN based HEMT devices have demonstrated outstanding potential for RF and power electronics applications. Although a tremendous improvement in the device performance has been achieved in recent years, it is still below the potential of what GaN material could offer. There is a strong demand to further enhance its performance, from its material quality to the device design and processing technology to meet the performance predicted by the materials figure of merit.

GaN HEMT structures can be grown on different substrates including sapphire, Si, SiC, diamond and GaN native substrate. While sapphire and Si substrates are the most cost-effective, better GaN HEMT's characteristics are achieved on SiC and GaN substrates. The advantage of the SiC over GaN substrate is its higher thermal conductivity, which can more effectively remove the heat generated by GaN components during high-frequency and high-power operations to enhance reliability. Encouragingly, a buffer-free GaN-on-SiC material known as QuanFINE has been developed by Swegan, one of partners within the UltimateGaN consortium. Besides the benefit of

thermal management, the QuanFINE material architecture functions excellently to block high voltages owing its AlN nucleation layer and the semi-insulating SiC (Si-SiC) substrate.

RISE has designed and fabricated different types of lateral normally-on HEMTs in wafer scale to validate and benchmark the QuanFINE structures grown on 4" Si-SiC substrate in comparison to GaN-on-Si epitaxy. The work has focused not only on verification of the high device performance but also on its yield for revealing its competitiveness in the cost-sensitive power electronics market. The fabricated HEMTs revealed the expected threshold voltage, good linearity with gate length and width, Ion/Ioff ratio of 10^8 as well as high output current up to 16 A with multiple fingers. The experimental outcome agrees well with the simulation results.

In addition to such wafer level HEMT device fabrication, we have also included different types of multi-finger HEMTs with designed electrodes for flip-chip soldering them into package modules produced by ceramic additive manufacturing (AM), also known as three-dimensional (3D) printing. The package design has aimed to address the stringent thermal and electrical requirements of these types of HEMTs for power electronic applications. Importantly the ceramic AM package design also enables the incorporation of intricate 3D features into the package structure for achieving increased electrical isolation distance between the source and drain contact pads of the HEMT in the package.

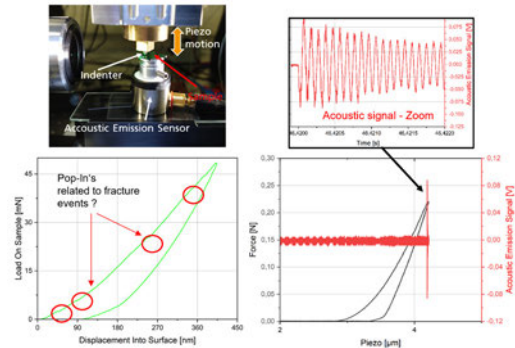
FAILURE DETECTION FOR BOND OVER ACTIVE APPLICATIONS BY ACOUSTIC EMISSION TECHNIQUES

LEAD PARTNER / AUTHOR:
Fraunhofer IMWS, Falk Naumann

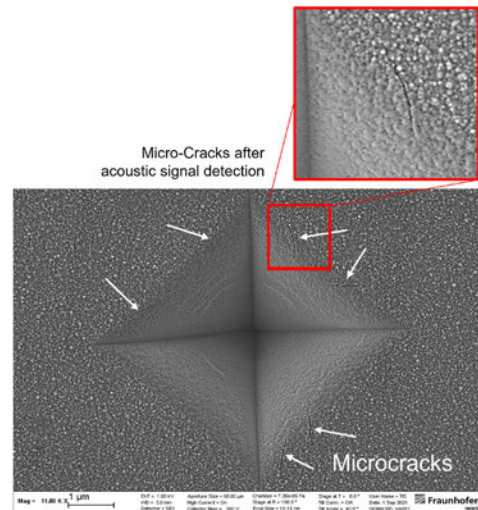
The combination of nano-indentation together with acoustic emission techniques allows the advanced strength characterisation of complex layer stacks for bond-over-active application at GaN devices.

During wire bonding of semiconductor devices, potential high mechanical stresses are locally introduced near the bond pad area. In order to validate the applicability and robustness of suitable BEOL buffer layer stacks for bond over active applications, appropriate test methods are needed. Within the UltimateGaN project Fraunhofer IMWS developed a nano-indentation approach combined with acoustic emission techniques to correlate measured pop-in events of the indentation experiments with microstructural damage (like the initiation of micro-cracks or delamination) allowing a robustness validation of BEOL stacks or to check their mechanical strength. Using this developed method, the detection of hidden micro-cracks underneath metallization layers becomes possible and supplements the measurement data (F-U-charts) of the indentation experiments by a further failure criterion. This approach was evaluated at various sample types / layer stacks from the UltimateGaN project partners and complemented by microstructural failure analysis using GHz-SAM and FIB/SEM cross section analysis. As a result, various mechanical stress conditions

– related to wire bonding processes – can be simulated by the indentation tools and surface hidden failures modes can be identified.



Test setup including the force-displacement (F-U) charts superimposed by the measured acoustic emission



SEM-image of the detected crack initiation at test substrates with passivation layers

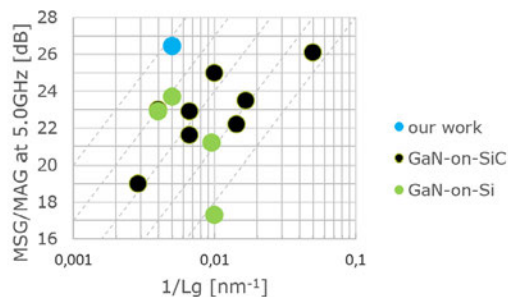
GAIN BEYOND STATE OF THE ART WITH GAN (ON SI) TECHNOLOGY

LEAD PARTNER / AUTHOR:
IFAG, Helmut Brech

New GaN on silicon RF power technology concept developed to deliver beyond state-of-the-art performance.

One of the most critical performance parameters for operating a high frequencies especially above 20GHz is the gain since the gain of any transistor is reduced with increasing frequency. For this reason, multiple gain stages are needed for most power amplifier applications at high frequencies. The required driver stages come with serious drawbacks of reduced overall efficiency and increased complexity and cost.

The gain of a transistor is typically increased by reducing the gate length and scaling other transistor parameters accordingly. Within UltimateGaN we have developed a new technology concept to push gain beyond current state-of-the-art when comparing gain for a given gate length. In the picture, the small signal gain MSG at 5GHz is shown versus the inverse of gate length ($1/L_g$). Our new GaN-Si technology concept is able to achieve the same gain as devices with the state-of-the-art technology concept but with up to an order of magnitude longer gate length, 200nm versus 20nm. Such high gain with a long L_g translates into very significant advantages such as high performance, high reliability and low cost due to manufacturability in a standard advanced silicon fab.



Small signal gain MSG at 5GHz versus $1/L_g$ for various GaN-Si and GaN-SiC HEMTs taken from literature and compared to our work within UltimateGaN

INNOVATIONS: PACKAGING

GAN EMBEDDING IN PCB

LEAD PARTNER / AUTHOR:

AT&S, Erich Schlaffer

Embedding of active and passive Components – a key feature for Miniaturization

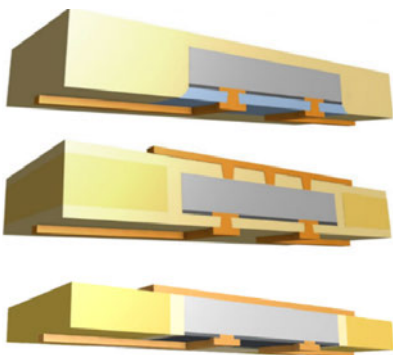
5G Active Antenna Systems (AAS) / Remote Radio units (RRU) is a core element of the Radio Access Network performing the over-the-air wireless link between User Equipment (UE) devices and the telecom network. Moving from the classical omnidirectional single antennas to complex antennas arrays allowing Massive MIMO digital beamforming creates the need for more complex, performing and power saving RF-Frontend integration in the RRU.

Antennas' size and heat dissipation are becoming more and more important for the full deployment of the 5G installations. The large PCBs used in discrete transceivers will be too large for massive MIMO arrays, where 64 or 128 antennas are arranged in close proximity to each other. Passive cooling is absolutely required for anything on a tower-top, and the

move to Massive MIMO greatly increases the number of radio paths. The possibility to offer Multi-Chip-Module System in Package (MCM SiP) RF power amplifiers, characterized by small form-factor, efficient power consumption and heat dissipation, is therefore cornerstone for the 5G deployment.

The proposed Central Core Embedding (CCE) technology, where active devices are embedded inside a multilayer laminate and contacted using laser vias, allows to produce miniaturized RF power amplifiers modules, outperforming surface mounted MCM SiPs in term of RF and thermal performance, while still offering 10X lower size than classical discrete transceivers on PCB solutions.

Compared to surface mounted active devices SiP, this approach minimizes the chip-to-matching-network interconnect parasitic components, allowing significantly larger bandwidth power amplifier designs, and reduces the thermal resistance from the module back-plate to the active chips, allowing improved thermal performance. Moreover, other signal conditioning and biasing chips of compatible thickness can be embedded as well, allowing further integration & footprint reduction of the power amplifier module.



Embedding of Bare Dies

ECP®

The first choice for cost-efficient packaging of passive and small-size active components
For low voltage applications (<50V)

CENTER CORE EMBEDDING

The preferred packaging technology for power applications with double-sided component connection

PARSEC²

The thinnest possible embedded package for active components with a wide range of metallization types

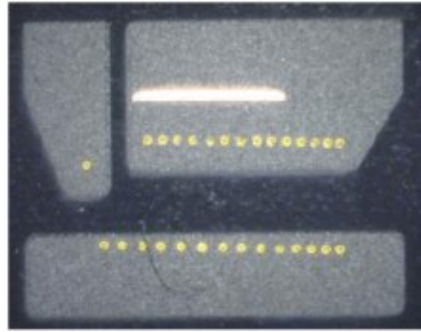
PLATEABLE MOLD PACKAGE FOR LOWEST R_{DSon}

LEAD PARTNER / AUTHOR:
IFAG / Stefan Wötzel

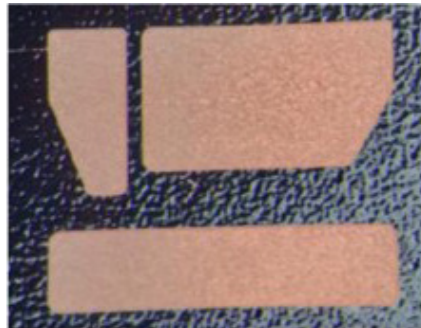
Integrated package solutions for high-voltage GaN are of particular interest. On the one hand, to realize integrated solutions with power device and Gate driver IC, for instance for power stages applications. On the other, the integration of several GaN power transistors to reduce a single switch's R_{DSon} becomes of interest for high-power applications, such as on-board chargers (OBC) for electrical vehicles (EVs). For both cases, a package technology with lowest parasitics is required to support the fast switching benefits of GaN transistor technology.

State-of-the-art semiconductor power packages rely on wire bonding or Cu clip-based technologies for the die's front side interconnect, associated with certain limitations regarding routing and electrical parasitics. An alternative approach for packaging and realizing the front side interconnect, based on an advanced epoxy mold compound technology, is considered here. By customized laser treatment (Laser direct structuring, LDS) of the mold body's surface, the chemical properties can be locally adjusted, enabling e-less plating of Cu layers on this surface. In a combination with Cu stud bumps applied to the die's pads, those plated Cu layers are used to form a low parasitic the front side interconnect. Additionally, the plated layers are utilized to re-route and fan-out the Source, Drain and Gate potentials on package-level.

The proposed concept for an integrated dual-die, low- R_{DSon} device utilizes this approach, benefiting from the lowest package parasitics (< 0.1 mOhm, < 0.1 nH) and well-adjusted interconnect length for Gate.



After LDS



e-less CU plating



ENIG plating

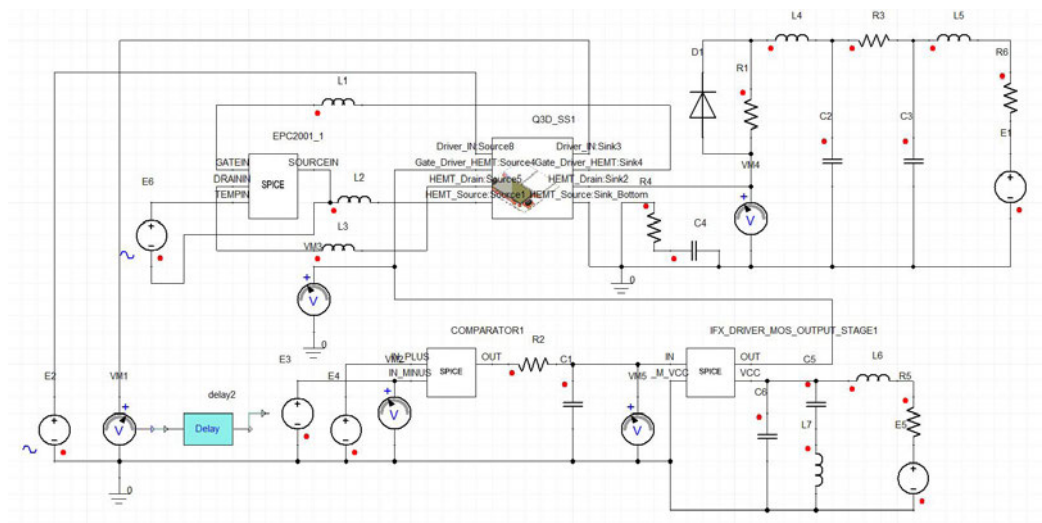
A SYSTEM IN PACKAGE FOR SHORTPULSE LIDAR

LEAD PARTNER / AUTHOR:

SAL, Thomas Moldaschl / IFAG,
Stefan Wötzel

Due to the specific operation profile of LiDAR for ADAS, the applied laser diodes need to be operated with short-pulsed currents of several tens ampere amplitude. Therefore, special GaN-based driver devices are needed fulfilling the demands accordingly. To ensure best performance, the semiconductor package needs to provide multi-die capability, low-level die-to-die interconnect and overall package parasitics. The package considered for this purpose is laminate-based. On this the GaN power transistor plus the associated, silicon-based Gate driver device are mounted in a flip chip configuration as close as possible together, reducing the decisive die-to-die interconnect parasitics from Gate driver output to Gate of the GaN power HEMT.

For this LiDAR system in package (SiP) a comprehensive multi-domain physical simulation is developed, incorporating electrical, thermal and mechanical effects of the LiDAR SiP. Optimizations in terms of electrical parasitics as well as thermal performance are performed on a theoretical level and are backed up by measurement results. In order to provide eye safety, as well as resolution requirements, the LASER pulses of the LiDAR system have to be kept in the nanosecond range. This infers current pulses in the same range, which are inherently limited by parasitic inductances in the power loop. Thus, the reduction of these parasitic inductances is of most importance, resulting in very short electrical connections. This small footprint however has the need to be properly cooled, which has to be performed on the same scale. Thus, thermal performance optimization and electrical performance optimization tend to result in a trade-off. All these factors are incorporated in a multi-domain physics simulation complemented by corresponding measurements.



LIDAR Schematics

INNOVATIONS: RELIABILITY

DISLOCATION TYPE DETERMINATION BY CATHODOLUMINESCENCE

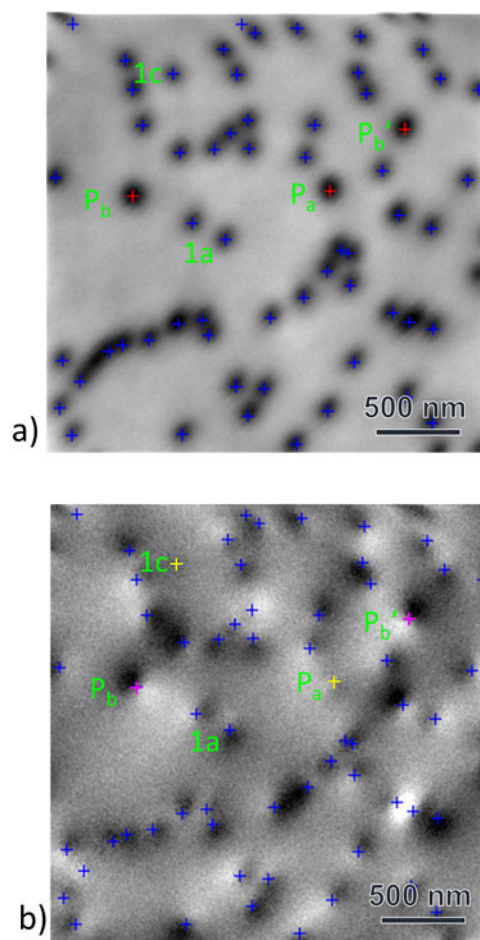
LEAD PARTNER / AUTHOR:

ATT, Marc Fouchier

Cathodoluminescence emerges as a reliable way of discriminating threading dislocations in a single, non-destructive step.

Threading dislocations (TDs) are extended defects present in most epitaxially grown GaN devices. They can roughly be categorized into edge and screw types. Screw dislocations can significantly impact device performance by acting as leakage current paths. Among the techniques for TD detection, transmission electron microscopy (TEM) can directly discriminate their type. However, it is slow and destructive. TDs manifest themselves as dark spots in cathodoluminescence (CL) intensity images. They also induce a strain field around them. The hydrostatic component of the strain manifests itself as a shift in the CL peak center energy. Simulations show that this strain field varies with the TD type. In particular, the strain around screw TDs has no hydrostatic component. However, the presence of TD pairs prevents from distinguishing screw TDs from the shift of the center energy alone. Figures a) and b) show maps of the CL intensity and peak center energy recorded on a GaN sample. TDs appear as dark spots on the peak intensity image. The most common spots, marked by a blue cross, have a weak intensity contrast and can be attributed to single TDs. A few TDs marked by a red cross, have a strong contrast and can be attributed to TD pairs. The crosses are reported on the peak center energy image where most fall in the mid-

dle of a butterfly structure that is characteristic of the hydrostatic strain around edge TDs. Two TDs however, marked by a yellow cross, induce little strain. From the intensity image, one of the two, labelled 1c, is a deleterious single screw TD. The 1a, Pa and Pb labels point to a single edge TD and two types of TD pairs. In summary, the combination of the intensity variation and the peak center energy variation around TDs emerges as a reliable way of discriminating them with CL in a single, non-destructive step.



CL a) intensity and b) peak center energy maps of a GaN sample

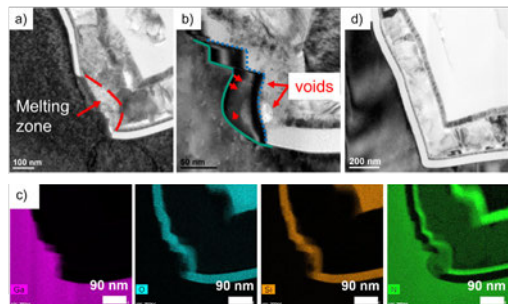
INNOVATIVE MICROSCOPY RESULTS FOR GAN RELIABILITY INVESTIGATION

LEAD PARTNER / AUTHOR:
Fraunhofer IMWS/ Frank Altmann
and Patrick Diehle

Advanced TEM investigation correlates a defect signature typical for gate isolation breakdown with structural irregularities of the gate trench.

Semi-vertical trench MOSFETs are intensively studied to enable high performance vertical devices. Related device structures and the development of required process modules are accompanied with novel reliability risks and failure modes. In this work we investigate gate shorts after reliability testing to identify their root cause and derive appropriated process improvements. Off-state step-wise electrical stress testing was applied on semi-vertical MOSFET devices until breakdown occurs and the failure position was localized by electroluminescence microscopy. As the EL spot is typically large compared to the real defect structure cross-sectional screening by focused ion beam (FIB) milling and scanning electron microscopy (SEM) observation followed by transmission electron microscopy (TEM) analysis was applied. Stepwise lamella thinning and TEM investigation started at approximately 1.5 μm lamella thickness containing the whole EL spot area down to approximately 50 nm thickness for optimal TEM imaging and analysis capability of the containing defect structure. Steep steps at the lower corners of the gate trench were found along the whole gate structure varying in shape and length. A defect structure as typ-

ical signature for electrical breakdown of gate isolation layer was observed at the lower edge of the gate trench. The defect structure is associated with a melting zone and the presence of several voids as result of the short current flowing. Detailed TEM analysis revealed, that the breakdown defect structure is associated with the presence of extra sharp steps. Additional EDX analysis of the defect, shows that the gate isolation breakdown led to a severe migration of nitrogen into the gate oxide and a minor migration of silicon and oxygen. A clear relation between breakdown of gate isolation and related defect signature could be identified as new failure mode. Based on these studies, the etch process to generate the gate structure was adapted. As the result of the process improvement newly processed devices without steep steps at the gate trench were fabricated with potentially higher breakdown voltage.



TEM analysis of defect at gate trench (a-c) and of gate trench after improving the process (d). a-b) BF-TEM images of approx. 100 nm and 50 nm thick lamella, c) chemical distribution maps of selected elements by EDX of 50 nm thick lamella, d) BF-TEM image of gate trench after process improvements

LASER ANNEALING FOR Mg- ACTIVATION IN P-GaN

LEAD PARTNER / AUTHOR:
UNIPD / Carlo De Santi

Excimer laser activation of Mg doping in gallium nitride can achieve electrical performance comparable to rapid thermal annealing, and it enables spatially-resolved activation.

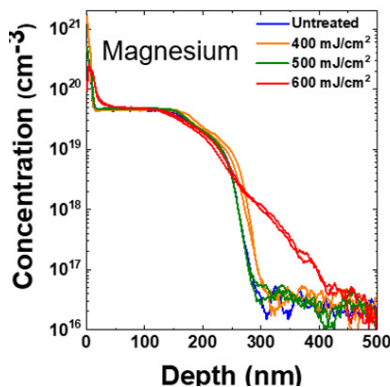
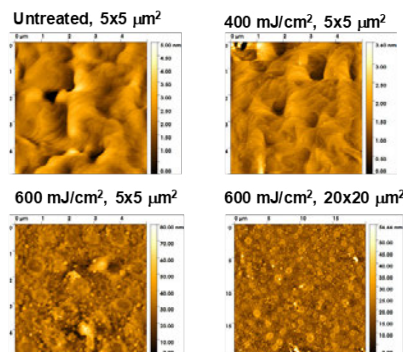
P-type doping in gallium nitride is a difficult task, due to the formation of magnesium-hydrogen complexes that effectively inactivate the Mg acceptor. For this reason, an additional step is needed in order to activate the acceptor by breaking the hydrogen bond, first demonstrated by low-energy electron beam irradiation (LEEBI) and then achieved by rapid thermal annealing (RTA) in nitrogen atmosphere at industrial level.

In the framework of the project, we investigated an additional method, the activation by irradiation with an excimer KrF laser (248 nm). This process has the advantage of allowing spatially-resolved activation, useful for the creation of carrier confinement regions.

The samples obtained by the first laser activation experiments have comparable resistivity with respect to the RTA samples, which were treated in highly optimized conditions. Temperature-dependent measurements confirmed that the conductivity originates from Mg activation, yielding an activation energy of 0.14 eV in agreement with the estimate for Mg acceptors in highly doped gallium nitride. In order to achieve the best performance,

repeated treatment with a large number of pulses at low energy densities is necessary.

Atomic force microscopy (AFM) measurements confirms that the morphology of the surface does not undergo any negative variation due to the laser treatment at the most effective activation condition, confirming the viability of this technique for the technological process. Time-of-flight secondary ion mass spectroscopy (TOF-SIMS) experiments show no back-diffusion of magnesium for moderate energy densities. Hydrogen is still detected in the sample and remains in the material even after the Mg-H bond is broken. Oxygen-rich surface layers can be found at the higher energy densities.



AFM measurements and TOF-SIMS experiments

ADVANCED RELIABILITY INVESTIGATION OF GAN MOS CAPACITORS

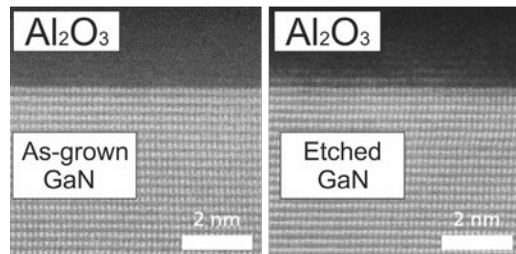
LEAD PARTNER / AUTHOR:

imec / Matteo Borga

Synergy between electrical and microstructural analysis to characterize MOS interface on GaN.

Gallium-nitride trench-gate vertical devices are of high interest in the field of power electronics because, unlike lateral architectures, they potentially allow to combine high breakdown voltage and reduced device footprint. These devices rely on a MOS (metal-oxide-semiconductor) gate structure, that hugely impacts the device performance and stability; a high-quality dielectric and dielectric-semiconductor interface are crucial to achieve low on-state resistance (high inversion channel mobility) and stable threshold voltage. Due to the complex device architecture, dedicated test structures were fabricated to analyze the materials and interface qualities. Planar MOS capacitors on as-grown GaN allowed to analyze the intrinsic potential of the materials structure by means of quantification of the dielectric trap density (CV-double sweep tests either in accumulation regime or deep depletion condition) and of the interface states density. Microstructural analysis was also performed employing HR-STEM and EDXS techniques, after an accurate sample preparation procedure based on large-area Ar-ion milling, proving the high quality of the materials and of their interfaces (see figure); an atomic flat interface was observed between the GaN and the dielectric. To evaluate the impact of the GaN etching process (needed for the formation of the final trench-gate device)

on the interface and dielectric quality, planar MOS capacitors on an etched GaN surface were fabricated. The same characterizations were performed as on the reference sample. Electrical-based tests showed a negligible variation of the dielectric trapping in accumulation regime, but an increased hysteresis when the structure is exposed to depletion-to-accumulation double sweep CV as well as a slightly increased interface states density. Microstructural analysis demonstrated that the etching process resulted in a few monolayer roughness of the GaN/dielectric interface, which is considered a remarkable achievement in terms of processing development. Lastly, trench-like capacitors allowed to study an eventual impact of the sloped sidewalls and of the topography formation. Lower dielectric breakdown voltage and TCAD simulations highlighted the presence of a non-uniform electric field within the dielectric along the trench, as it is crowding at the trench corners. Moreover, interface states density resulted to be higher than in the other structures, thus indicating either a worsening of the trapping favored by the locally increased electric field, or the impact of the different crystal planes involved, leading to a different amount of damage in the planar and diagonal region of the trench.



HR-STEM - Atomic flat interface between the GaN and the dielectric

INNOVATIONS: APPLICATIONS

SMART GRIDS: SINGLE-PHASE PV INVERTER

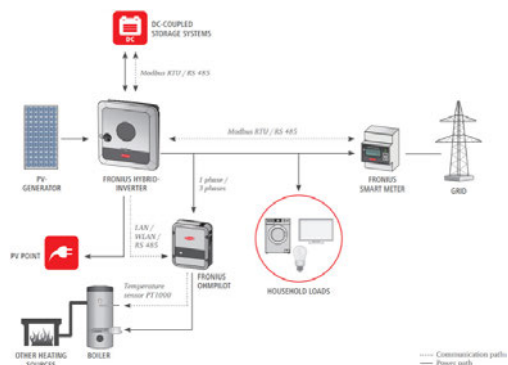
LEAD PARTNER / AUTHOR:
Fronius / Philipp Rechberger

UltimateGaN helps us to further increase the efficiency of PV inverters and therefore supports the energy transition.

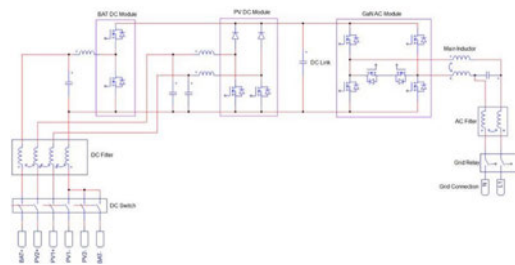
Solar energy is one of the key players in renewable energy production. Nevertheless, Photovoltaic (PV)-modules produce only direct current (DC) from sunlight which is why an inverter is needed to convert the energy into grid-compatible AC. The goal of Fronius within the Ultimate-GaN project is to develop a fully-GaN 10 kW single phase PV inverter for residential applications with battery storage capability. Due to longer operating-times in part load in PV-battery systems an increase of the part load efficiency is one of the two main objectives of T6.3.1. Additionally, based on the characteristics of GaN the power density of the inverter system should be increased by higher switching frequencies.

As a basis for the inverter system an advantageous power electronics topology was selected. The focus was laid on overall efficiency and filtering effort compared to other topologies as well as extensive experience with the setup. One of the core aspects of this demonstrator is, that the whole switching topology is built up within a power module which was developed together with project partner Infineon Austria. The use of power modules has significant advantages regarding the design and cooling of the device. On the other hand, more effort is required in terms of gate-driver design and positioning.

By optimisation of switching frequency, dead time and gate-driver design an efficient overall operation could be achieved. Efficiency simulations carried out at the beginning of the project could be confirmed by first measurements. With the use of GaN a significant increase of efficiency especially in part load conditions as well as a rise in power density of the device compared to standard Si/SiC power electronics is possible.



Fronius system overview



Simplified inverter schematics

SMART GRIDS: HIGH EFFICIENCY DC MICROGRIDS BASED ON GAN

LEAD PARTNER / AUTHOR:
FORES / Jorge Herrero

More than 3000 hours of field tests demonstrate how GaN devices show best reliability and low losses in class, enabling a new generation of green, efficient power electronics converters.

Do you know what an electrical microgrid is? A microgrid is a group of at least two different electrical generation sources with lower power ratings than conventional power plants, which work together in order to cover the electricity demands of several consumers, independently of their degree of connection to the public electricity grid. This electricity distribution scheme has been brought to light by the rise of renewable energies, specially wind and PV but also storage, and will contribute towards reaching the desired objectives of affordable and clean electrical energy, for all.

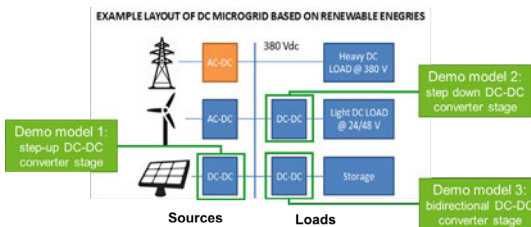
An example of simple microgrid is a PV plant with battery storage which feeds a small isolated farm; another example would be a remote village where houses, commerce and industry are powered through a complex mix of wind turbines, PV power, hydro generators, hydrogen power and batteries.



In microgrids, power electronics take a critical role: since the power sources work with different voltages, frequencies and type of current (some are DC, others AC) the role of power electronics is to convert the energy generated by each power source, to the tight, specific conditions it needs to be used by end consumers. Without them, a microgrid concept would not work as such.

During UltimateGaN, FORES has been focused on developing all stages needed to integrate PV, wind and storage in a novel concept known as “DC microgrid”, which has the potential to reduce the cost and increase the efficiency of such microgrids, playing our part for a better, greener future. 3 different models of low cost, modular DC-DC converter up to 5kW were developed, reaching efficiencies up to 98.4%. This converter concept has the potential to be widespread in renewable energy applications such as PV, storage, hydrogen... and has been already tested successfully in the field for more than 3000 hours.

The key to achieve such good results: our core know-how on DC-DC converters, the usage of automatic design algorithms developed in-house to optimize transformers and all components, and of course the outstanding performance of the GaN devices developed in UltimateGaN!



Examples of simple microgrids

SMART MOBILITY: LIDAR

LEAD PARTNER / AUTHOR:

IFI / Maurizio Galvano, Alessandro Scanferla

LIDAR is the most attractive and efficient solution to help an autonomous vehicle to understand the world around it.

The focus of this activity is fully autonomous self-driving car, and in particular what helps an autonomous vehicle to understand the world around it.

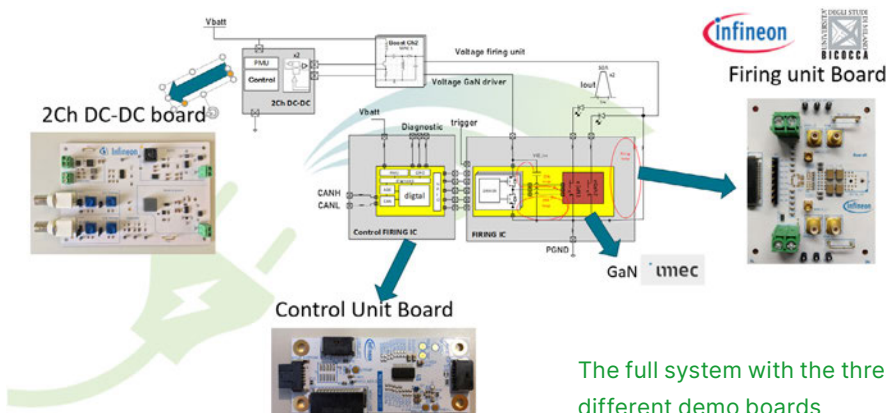
LIDAR application is the most attractive and efficient solution for this market. The challenges of LIDAR consist in the development of the electronics generating a current pulse of ca 50A that lasts for less than 5ns, with rise and fall times in the order of less than 1-2 ns. Depending on the LIDAR application software, it is also required to repeat the pulses with a defined firing frequency and to sequence the pulses with the right timing. GaN is an ideal candidate to serve this application due to the superior switching performances with respect to Silicon power transistors. Therefore, there is the need for a multichannel GaN Driver IC able to drive multiple GaN transistors

with the required speed, one control unit IC able to communicate with external uC and configure the GaN Driver to deliver the required pulses and finally a two channels DC-DC able to supply the control IC the Driver IC and provide variable voltage to the Laser diode.

Infineon and UniMiB developed three different ICs with related PCB boards to meet all defined requirements. All IC's were designed to fulfill automotive qualification and ready to be productive.

During the PCB's design phases special attention was put on the Firing Unit Board that has to provide very high current pulse (up to 50A) to the laser diode within 5ns time. Due to this stringent current requirement we had to reduce at the minimum the parasitic elements using a dedicated tool and board layout method to optimize the design.

The designed board layout is exported to ANSYS SIWAVE, extracted element were used as input for ANSYS Q3D to calculate the parasitic component values, simulate the effect on our circuit and improve it. Several iterations of such a flow allowed to find the optimum layout to meet the current pulse requirement.



The full system with the three different demo boards

SMART MOBILITY: WIRELESS BATTERY CHARGER

LEAD PARTNER / AUTHOR:
IKERLAN / Asier Garcia

GaN-based wireless battery charger results on an integrated pluggable low-profile and high efficient design that avoids the use of an external wallbox for the power converter, simplifying the connection between power stage and inductive coils, and approaches the typical efficiency of a plug-in battery charger (<95%).

Currently, wireless technology is moving from low power to higher power applications. The lack of wires has several advantages in electric vehicle charging systems, such as no need to carry bulky charging cables in the car, more comfortable for the end user, safety due to less human action required, maintenance-free, immunity to dirt and water, or the possibility of avoiding vandalism. However, there are currently also some challenges related to the complexity of the charging system, the standardization, and a lower efficiency of the whole charging system.

During UltimateGaN project, a high-efficiency low-profile bidirectional 3.6kW wireless battery charger has been developed, based on last-generation gallium nitride (GaN) devices and a novel power-electronics single-stage topology. The coil and the power converter have been integrated in a unique housing avoiding the wallbox and an extension of the high-frequency cable, and simplifying the wireless charging system. A low height power converter (below 14mm) has been designed including all

elements except the wireless coil and ferrites, i.e., the power PCB, control board, all electronics components, connectors, power supplies and cooling system. The battery charger operates at 85kHz frequency, fulfilling the automotive standard J2954. A high efficiency of the whole battery charger system (above 95 %) has been achieved, including all losses and consumption, thanks to the novel topology and low losses of the GaN devices.

The main characteristics are summarized:

- A 3.6kW 85kHz wireless battery charger based on automotive standard J2954.
- GaN HEMT semiconductor technology.
- Transmission distance up to 100mm.
- Ultra-compact design with a low-profile power converter.
- Integration of wireless coil and converter in a single housing, avoiding a wallbox.
- Power factor correction, bidirectionality and battery voltage and current controls included.
- High-efficiency (>95%) wireless charger system.



Wireless battery charger with an electric vehicle

SMART MOBILITY: NEXT GEN ON BOARD BATTERY CHARGER USING GAN TECHNOLOGY

LEAD PARTNER / AUTHOR:
LEAR Corporation / Rafael Jiménez /
/ Antoni Ferré

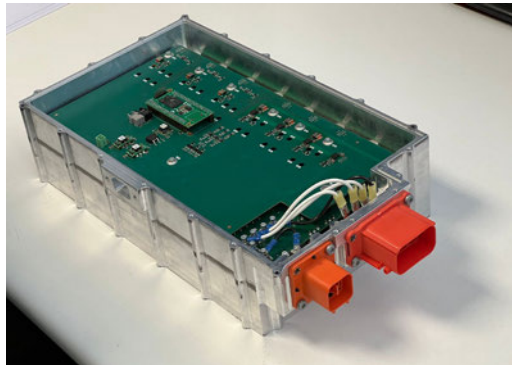
Thanks to the 40 mΩ GaN devices developed by Infineon, LEAR CORPORATION has managed to build the PFC as single branch and the DCDC as a full bridge instead of a half-bridge, reducing the number of active components required and improving notably the power density of the On-Board Battery Charger.

LEAR Corporation has contributed to Ultimate-GaN Objective 6 (demonstrate European leadership in high performance power electronics and RF application domains) developing and implementing an On-Board Charger (OBC). The OBC is the system built into the car to recharge the high voltage battery from the AC grid while the vehicle is parking. Current trends include increasing the conversion efficiency and the power density for better energy efficiency. The OBC developed uses a dual stage topology with a totem-pole bridgeless PFC and a dual-active bridge DC/DC converter. Thanks to the 40 mΩ GaN devices developed by Infineon, it has been possible to build the PFC as single branch and the DCDC as a full bridge instead of a half-bridge and reduce the number of active components required.

Experimental results are very satisfactory. It was achieved operation at much higher frequencies compared to Si or SiC. Correspondingly, the size of magnetics has been reduced ~25%. The OBC also shows increased efficiency respect cur-

rent generation commercial OBCs for full load operation. A final optimized version with power efficiency >96% and power density >2,5 Kw/l is currently being designed.

- Topology selected is a dual stage with totem-pole bridgeless PFC and a dual-active bridge DC/DC converter
- Thanks to the 40 mΩ GaN devices developed by Infineon, it has been possible to build the PFC as single branch and the DCDC as a full bridge instead of a half-bridge and reduce the number of components
- Experimental results show that operation at much higher frequencies compared to Si or SiC are achievable
- Due to high frequency operation, the size of magnetics has been reduced ~25%.
- Increased efficiency respect current SotA for full load operation and increased power efficiency (~96%)
- Power density ~ 2,5 kW/l



OBC prototype

5G: 2KW/48V IP65 GAN RECTIFIER FOR 5G APPLICATION

LEAD PARTNER / AUTHOR:
Eltek AS / Odd Roar Schmidt

GaN is the future for
Telco and Datacenter power.

GaN transistor used in totem pole topology for PFC:

- Totem pole topology gives very high efficiency
- GaN transistor together with all other semiconductor uses the IP65 box as heatsink.
- No internal fans
- Mounting method of semiconductors in the IP65 box ensure constant pressure for optimized heat transfer.
- At least 35degC margin on the GaN transistor chip at + 55degC ambient ensure very good reliability.

Reliable operation:

- Totem pole topology with GaN transistor are modified to give very reliable and robust performance with overcurrent, voltage and current limitation with respect power loss during those operation conditions.
- Very high peak efficiency, 97,8% together with very good thermal performance ensure safe operation at low input voltage, high input current and low output voltage with high output current, which maximum power loss at +55degC ambient

State of the art:

- The IP65 GaN rectifier has demonstrated following;
- Peak Efficiency of 97,8%
- Very low cost
- Low weight 3,6kg
- Very small outer dimensions
- Pluggable IP65 rectifier
- +55degC operation with very good temperature margin on all semiconductors



2kW/48V IP65 GaN rectifier for 5G application

5G: AFFORDABLE 5G-AMPLIFIERS ENABLING A FASTER 5G ROLLOUT

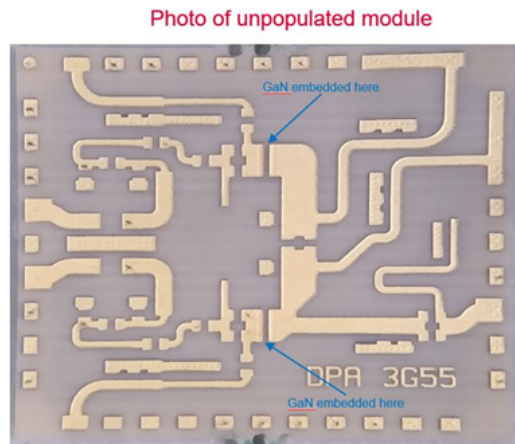
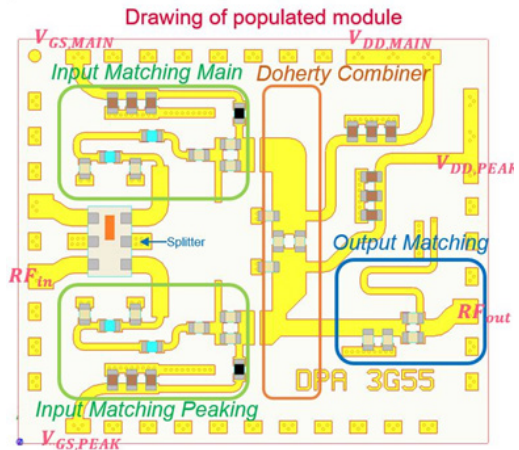
LEAD PARTNER / AUTHOR:
TU Graz / Helmut Paulitsch

UltimateGaN designed a GaN on Silicon RF power amplifier for 5G applications with outstanding efficiency and bandwidth.

With the development of future 5G wireless communication networks, there is an increasing use of array antennas in base stations to allow adaptive beamforming and multiple independent beams. These array antennas consist of many independent radiating elements, each driven by a small power amplifier module (PAM). To allow a high integration density with many radiating elements a small footprint is required, as well as a high efficiency to cope with limited heat dissipation capabilities (passive cooling).

Supporting these requirements, UltimateGaN has developed a sub 6 GHz PAM based on Infineon GaN on Silicon transistors in a Doherty amplifier architecture. The developed PAM can deliver 40 W peak output power with an average output power of 5W at 45% efficiency over a unprecedented instantaneous bandwidth of 800 MHz in the frequency range of 3.1 to 3.9 GHz. The module use chip embedding technology to integrate the GaN transistors in the module's PCB stackup, resulting in a small footprint of 10 × 11 mm.

The performance of the UltimateGaN GaN on Si based PAM is close to GaN on Silicon Carbide technology based solutions, but can be produced at much lower cost, thus enabling an affordable 5G rollout.












5G power amplifier module, drawing and photo

CONTRIBUTORS

The UltimateGaN consortium consists of 26 well-established participants originating from 9 European member states and associated countries, constituting a balanced mix of industry and research with complementary skills and expertise. The multidisciplinary partners cover the entire value chain technology – packaging – reliability – application.

LOGO	PARTICIPANT ORGANISATION NAME	SHORT NAME	COUNTRY	ADDRESS
	Infineon Technologies Austria AG	IFAT	Austria	Siemensstraße 2, 9500 Villach
	Fronius International GmbH	Fronius	Austria	Froniusstrasse 1, 4643 Pettenbach
	Silicon Austria Labs GmbH	SAL	Austria	Europastraße 12, 9524 Villach
	Technische Universität Graz	TUGraz	Austria	Rechbauerstrasse 12, 8010 Graz
	Austria Technologie & Systemtechnik Aktiengesellschaft	AT&S	Austria	Fabriksgasse 13, 8700 Leoben
	IMEC	IMEC	Belgium	Kapeldreef 75, 3001 Leuven
	AIXTRON SE	AIX	Germany	Dornkaulstraße 2, 52134 Herzogenrath
	Infineon Technologies AG, Regensburg	IFAG	Germany	Am Campeon 1-15, 85579 Neubiberg
	Siltronic AG	SAG	Germany	Hanns Seidel Platz 4, 81737 Munich

LOGO	PARTICIPANT ORGANISATION NAME	SHORT NAME	COUNTRY	ADDRESS
	Max-Planck-Institut für Eisenforschung GmbH	MPIE	Germany	Max Planck Strasse 1, 40237 Düsseldorf
	Fraunhofer Gesellschaft zur Förderung der angewandten Forschung e.V.	Fraunhofer	Germany	Hansastrasse 27C, 80686 München
	Technische Universität Chemnitz	TUC	Germany	Strasse der Nationen 62, 09111 Chemnitz
	NaMLab gGmbH	NaMLab	Germany	Nothnitzer Strasse 64, 01187 Dresden
	Università degli studi di Padova	UNIPD	Italy	Via 8 Febbraio 2, 35122 Padova
	Infineon Technologies Italia Srl	IFI	Italy	Via Die Valtorta 48, 20127 Milano
	Università di Milano Bicocca	UniMiB	Italy	Piazza dell'Ateneo Nuovo, 20126 Milano
	Eltek AS	Eltek	Norway	Graterudveien 8, 3036 Drammen
	Slovak University of Technology in Bratislava	STUBA	Slovakia	Vazovova 5, 81243 Bratislava

LOGO	PARTICIPANT ORGANISATION NAME	SHORT NAME	COUNTRY	ADDRESS
	Nano Design SRO	Nano	Slovakia	Drotarskacesta 6385 19A, 81104 Bratislava
	Ecole Polytechnique Fédérale de Lausanne	EPFL	Switzerland	Batiment CE 3316 Station 1, 1015 Lausanne
	Attolight SA	ATT	Switzerland	EPFL Innovation Park Building D, 1015 Lausanne
	IKERLAN S COOP	IKERLAN	Spain	P Jose Maria arizmendiarieta 2, 20500 Mondragon
	For Optimal Renewable Energy Systems SL	4Fores	Spain	Calle Celsa 17 Nave 13A, 50197 Zaragoza
	LEAR Corporation Engineering Spain Sociedad Limitada	LEAR	Spain	C/ Fusters 54, 43800 Valls
	RISE Research Institutes of Sweden AB	RISE	Sweden	Brinellgatan 4, 50115 Boras
	SweGaN AB	SweGaN	Sweden	Olaus Magnus väg 48A, 58330 Linkoping

IMPRINT

PROJECT COORDINATOR:

Herbert Pairitsch

Lisa Zernig

Infineon Technologies Austria AG

Siemensstraße 2

A-9500 Villach

Austria

UltimateGaN@infineon.com

OWNER, PUBLISHER AND RESPONSIBLE FOR CONTENT:

UltimateGaN project partners

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DESIGN:

MgA. Michaela Nerudová

PRODUCTION:

MgA. Jano Kaločaj

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